数字部分 实验二 逻辑综合与等价性检查

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思考题

(1) 将2.5节中打开阅读的时序库文件对应的PVT信息填入表格中。

|  |  |  |  |
| --- | --- | --- | --- |
| 时序库文件名 | 工艺角 | 电源电压 (V) | 温度 (℃) |
| **fast\_vdd1v0\_basicCells.lib** | 1 | 1.1 | 0 |
| **slow\_vdd1v0\_basicCells.lib** | 1 | 0.9 | 125 |

(2) 将2.5节中逻辑综合各阶段得到的电路基本信息填入表格中。

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 综合阶段 | **elaborate** | **syn\_generic** | **syn\_map** | **syn\_opt** |
| #Leaf Cells | 50 | 37 | 22 | 21 |
| #Terms | 10 | 10 | 10 | 10 |
| #Nets | 36 | 39 | 24 | 24 |
| #StdCells | 9 | 37 | 22 | 21 |
| 电路单元名称 |  |  |  |  |

(3) 从2.6节生成的报告中，找出以下数据并填入表格中。

**report\_timing命令运行结果中的部分数据**

|  |  |
| --- | --- |
| **Critical Path** | **Value** |
| **Group** | clk |
| **Start Point** | (R) count\_reg[0]/CK |
| **End Point** | (R) count[0] |
| **Clock Edge (ps)** | 10000 |
| **Output Delay (ps)** | 1000 |
| **Require Time (ps)** | 9000 |
| **Data Path Delay (ps)** | 316 |
| **Slack (ps)** | 8684 |

**report\_power命令运行结果中的部分数据**

|  |  |
| --- | --- |
| **Item** | **Value** |
| **Instance** | counter |
| **Cells** | 21 |
| **Leakage Power (nW)** | 1.544 |
| **Dynamic Power (nW)** | 3921.389 |
| **Total Power (nW)** | 3922.933 |

**report\_qor命令运行结果中的部分数据**

|  |  |
| --- | --- |
| **Item** | **Value** |
| **Clock Period (ps)** | 10000 |
| **Critical Path Slack (ps)** | 8684.3 |
| **Total Negative Slack (TNS) (ps)** | 0 |
| **Sequential Instance Count** | 8 |
| **Combinational Instance Count** | 13 |
| **Total Area (um2)** | 72.504 |
| **Max Fanout** | 8(clk) |
| **Min Fanout** | 0(rst) |
| **Average Fanout** | 2.3 |

(4) 从5.4节生成的报告中，找出以下数据并填入表格中。

**set system mode lec命令运行结果**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Mapped points: SYSTEM class** | | | | |
| **Mapped points** | **PI** | **PO** | **DFF** | **Total** |
| **Golden** | **2** | **8** | **8** | **18** |
| **Revised** | **2** | **8** | **8** | **18** |

**compare**命令运行结果

|  |  |  |  |
| --- | --- | --- | --- |
| **Compared points** | **PO** | **DFF** | **Total** |
|  | **8** | **8** | **16** |

**report verification**命令运行结果

|  |  |
| --- | --- |
| **Verification Report** | |
| **Category** | **Count** |
| **1.** **Non-standard modeling options used:** | **0** |
| **2.** **Incomplete verification:** | **0** |
| **3.** **User modification to design:** | **0** |
| **4.** **Conformal Constraint Designer clock domain crossing checks recommended:** | **0** |
| **5.** **Design ambiguity:** | **0** |
| **6.** **Compare Results:** | **PASS** |

要求：思考题解答以电子版形式发给数字设计助教老师，文件名为：学号+姓名。